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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/623,983	07/21/2003	Zhijian Xie	3-4	5529

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EXAMINER	
ABRAHAM, FETSUM	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 11/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/623,983	XIE ET AL.	
	Examiner	Art Unit	
	Fetsum Abraham	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *the rest* is/are rejected.

7)☒ Claim(s) *12 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Final rejection

DETAILED ACTION

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 9 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are: the vertical DMOS structure in claim 9 within the lateral DMOS structure of claim 1. There is clearly a physical shift of certain degrees between the lateral and the vertical LDMOSs in claim 1 and claim 2. In view of the structural shift, said shielding structure would have to shift like wise to consistently fit into its position as claimed in claim 1 (between the gate and the second source/drain region) which would mean that it would have to be buried in the substrate to say the least. Furthermore, the wiring specifics of claim 1 such as the "vertical conductor" in a "region of the device overlying the active area" would no longer apply to the vertical structure of claim 9.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 5-8,14,15,16 are rejected under 35 U.S.C. 102(a) as being anticipated by Morikawa et al (6,707,102).

As for claims 1,6,7,8,14,16 the patent discloses a power LDMOS device in the front page comprising a first conductivity type semiconductor substrate (1), first source/drain region (5), second source/drain region (9) spaced apart from the first source/drain region, a gate (3) proximate an upper surface of the substrate at least partially between the first and second source/drain regions, a shielding structure (10) proximate the upper surface of the substrate and between the gate (3) and the second source/drain region (9), the shielding layer at least partially electrically connected to the first region (5) by way of connection comprising substantially vertical conductor formed in a region of the device overlying an active area (an area bounded between the source/drain regions 5 and 9) and specifically between the gate (3 and the second source/drain region (9), the shielding structure being laterally spaced apart from the gate (3) and being non-overlapping relative to the gate.

As for claims 2,3,15 the conductive trace formed by metallization process connecting the shield structure and the first source/drain region is spaced apart from the gate by an insulation layers (12,22). Please note that any process that forms metal contact in a semiconductor structure involves metallization process.

As for claim 5, at least (12), one of the insulation layers separating the gate from the shield structure is oxide.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4,10,11,13,17, are rejected under 35 U.S.C. 103(a) as being unpatentable over Morikawa et al (6,707,102).

As for claim 4, a multilayered contact through vias or feedthroughs is a common practice in MOSFET contact technology. Such contact structures are used because they provide well insulated contact structures and provide easier access for electrical signal applications at the highest level of MOSFET topology. Therefore, it would have been obvious to use a multilayered contact in the MOSFET of the prior art for the advantage such contacts provide to such structures.

Although PN: 5,470,791, fig. 7N is provided to support the analysis, **"product by process"** claims are directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685 and In re Thorpe, 227 USPQ 964, 966. Therefore, the way the product was made does not carry any patentable weight as long as the claims are directed to a device. Further, note that the applicant has the burden of proof in such cases, as the above case law makes clear. Also see MPEP 2113.

As for claims 10,17, the prior art's shielding layer position and that of the claimed invention are identical. See the structure in the front page of the prior art and that in the one provided in figure 2 of the Application for reference. Also note that the insulation layers separating the shielding structures from the drain regions are thicker than the gate insulation layers used in the structures. Further, please note that the elevation of the shielding structures in relation to the position of the gate in vertical orientation is similar in both structures. Clearly, the lateral spacing difference between the gate and the shielding layer in both structures if there is one is immaterial so far as capacitance is concerned because the shielding layer is positioned on the drain region in both structures. Therefore, the prior art inherently reads to any type of capacitance issues raised by the claimed invention including the phrasing "without substantially increasing a capacitance between the gate and the first source/drain region" in the claim.

Furthermore, the examiner stands solid on the past position that the shielding layer has no effect on the capacitance formed between the gate end the first source/drain region of the structure since it has no effect on the constant position of the gate electrode in relation to the first source/drain region.

As for claim 11, the size of a "plug" can be controversial but any conductor formed through a via is a conductive plug from broad view definition. Although the current application omits to provide its perspective definition of a plug, assuming a plug meaning a relatively high volume conductive in a via, the prior art at least shows such a contact structure in relation to the conductors

(20,15,13)). A plug in relation to the shielding layer (10) may be missing from the prior art, but, it would have been obvious to one skilled in the art to use such contact means since they provide more current paths compared to thinner conductors.

As for claim 13, interlayer (22) is formed on the upper surface of the DMOSFET and the contact structure, a small plug depending on wide range definition of the term passes through that insulation layer to make contact with the shielding structure (10).

Claims 12 and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Examiner's answer to applicant's argument

The argument that the prior art does not show a shielding structure proximate the upper surface of the semiconductor layer between the gate and the second source/drain region has been considered but found unrealistic in view of the prior art front page structure. This feature is also very well discussed in the action above.

The connection and wiring structures relating the first source/drain region and the shielding structure was also considered but found moot in view of the prior art front page structure. This feature is also very well discussed in the action above. The argument related to the field oxide layer of the prior art is in fact not part of the action at all. That particular contact relates to the gate and layer (14) not to the shielding layer (10) and the first source/drain region. Therefore, the examiner considers the argument irrelevant to essence of examination based on the claimed structure because no shielding structure (10) is connected to the gate or to layer (14) in the prior art.

As for the argument in relation to the capacitance in view of the existence of the shielding layer, details are provided in the action and the prior art's silence on the capacitance issue does not mean there is no capacitance emanating because of the shielding layer. That capacitance in relation to the gate and the second source/drain region is unavoidable and it exists with similar effect to that in the claimed invention. Therefore, the argument is again found to be moot.

As for the argument in relation to claim 9, lateral and vertical MOSFETs are completely different devices structurally. Therefore, a shielding layer formed between gate and second source/drain region of a lateral MOSFET can not be structurally defined as such in a vertical MOSFET without positional adjustment in vertical orientation. Therefore, the shielding layer's position in the lateral MOSFET raised an omit ion of essential element, amounting to a gap between the elements, the elements being the gate, the source and drain regions, the insulation layers, the wiring and contact structures and the overall active layer of the MOSFET to say the least.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fetsum Abraham whose telephone number is: 571-272-1911. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915.

Fetsum Abraham
11/8/05